Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **DIR**
2. **A1**
3. **A2**
4. **A3**
5. **A4**
6. **A5**
7. **A6**
8. **A7**
9. **A8**
10. **GND**
11. **B8**
12. **B7**
13. **B6**
14. **B5**
15. **B4**
16. **B3**
17. **B2**
18. **B1**
19. **N. OE**
20. **VCC**

**3 2 1 20 19 18**

**8 9 10 11 12**

**17**

**16**

**15**

**14**

**13**

**4**

**5**

**6**

**7**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .003” X .003”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .065” X .066” DATE: 11/15/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HC245**

**DG 10.1.2**

#### Rev B, 7/19/02